ROLL NO. _____

Code: AE74/AE122/AC122 **Subject: VLSI DESIGN**

AMIETE – ET/CS (Current & New Scheme)

Time: 3 Hours **June 2018** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. Which one has highest power consumption?
(A) ECL **(B)** CMOS
(C) NMOS **(D)** GaAs

b. Which technology offers lowest delay?
(A) Bi-CMOS **(B)** CMOS
(C) NMOS **(D)** GaAs

c. What is relative permittivity for silicon dioxide?
(A) 8.85 **(B)** 10
(C) 8 **(D)** 4

d. What is the range for MSI?
(A) 10 **(B)** 100-1000
(C) 1000-20000 **(D)** 100000

e. The $Z_{P.U.}/Z_{P.D}$ for an inverter driven by an inverter
(A) 4 **(B)** 2
(C) 8 **(D)** 16

f. For n inputs in a Wallace tree the adder cell grows like
(A) $\log_2(1/n)$ **(B)** $\log_2(n)$
(C) $\log_{10}(n)$ **(D)** None of these

g. Which stick diagram from following Device uses two Polysilicon layers?
(A) nMOS **(B)** CMOS
(C) Both **(A)** & **(B)** **(D)** BiCMOS

h. Which circuits are susceptible to latch up problems?
(A) nMOS **(B)** pMOS
(C) BiCMOS **(D)** CMOS

i. Which model is suitable to represent a "stuck-at" fault?
(A) Mathematical model **(B)** Physical Model
(C) Logical Model **(D)** None of these

j. RC delay _____ when line width becomes smaller?
(A) Increases **(B)** Decreases
(C) No Change **(D)** Can't Say

Answer any FIVE Questions out of Eight Questions.
Each question carries 16 marks.

Q.2 a. What is a BiCMOS technology? Compare BiCMOS and Bipolar technologies. **(6)**

b. Describe the process for CMOS fabrication using n-well process. **(10)**

Q.3 a. Give Aspects of MOS transistor threshold voltage. **(4)**

b. In an nMOS transistor operating at room temperature following measurements are done V_{GS}=4V V_{SB}=2.6V V_{DS}=4V I_D=144μA and the process parameters are W/L=1, t_{ox}=400Å, $|2\Phi_F|$ = 0.64 V & $N_A=10^{16}/cm^3$. Find V_{th}, electron mobility and body effect coefficient. Assume oxide charge Q_{OX}=0 **(8)**

c. Derive the drain current vs voltage characteristics. **(4)**

Q.4 a. Draw a symbolic diagram for 1- bit CMOS shift register. **(4)**

b. Explain lambda- based design rules for nMOS, pMOS and CMOS transistors. **(8)**

c. Discuss the role of layout in VLSI circuits. **(4)**

Q.5 a. What is sheet resistance? Find expression for standard unit of Resistance for MOSFET. **(6)**

b. Explain delay unit. Estimate the rise time and fall time of a CMOS. **(10)**

Q.6 a. Discuss Parity generator circuit of a basic one-bit cell using stick diagrams. **(6)**

b. Discuss Pseudo-nMOS, Dynamic, and Clocked CMOS Logics in detail. **(10)**

Q.7 a. Explain working of a Carry look ahead adder. **(10)**

b. Using an example implement ALU function with an adder. **(6)**

Q.8 a. Discuss the design of a pseudo-static RAM cell. **(6)**

b. Explain all ground rules for a successful design. **(10)**

Q.9 a. Discuss how to test a combinational logic. **(8)**

b. Explain the uses of a CIF code. **(8)**